Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	(signaling pattern generator AND bit lines AND bus AND MUX AND selector AND switch AND linear feedback shift register AND LFSR AND signals AND memory chip AND processor AND bit pattern AND data pattern AND signal pattern).clm.	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/03/31 18:18
L3	215663	generat\$3 same (signaling pattern\$1 or signal\$1 or data pattern\$1 or data signal\$1 or signal pattern\$1) same (processor\$1 or LFSR\$2 or decoder\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:21
L4	62187	(select\$3 or multiplex\$3 or MUX or switch\$3 or control\$4) same (first group\$1 same first bit pattern\$1 or first bit line\$1 or first data pattern\$1 or first signal\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:24
L5	9419	I3 and I4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:24
L6	65736	(select\$3 or multiplex\$3 or MUX or switch\$3 or control\$4) same ((second group\$1 or remaining group) same second bit pattern\$1 or second bit line\$1 or second data pattern\$1 or second signal\$1 or remaining bit line\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:26
L7	6733	I5 and I6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:29
L9	1357	generat\$3 and ((signal\$1 or data pattern\$1 or pattern signal\$1 or signaling pattern\$1) same (feedback ship register\$1 or LFSR\$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:30

L10	35	17 and 19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON .	2007/03/31 18:29
L11	172018	transmit\$4 and ((signal\$1 or data pattern\$1 or pattern signal\$1 or signaling pattern\$1) same (bit line\$1 or remaining bit line\$1 or selected group or bus\$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:31
L12	. 12		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:32
L13	42526	memory chip\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:32
L14	308892	decoder\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:32
L15	1111439	processor\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:32
L16	4971	I13 and I14 and I15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:32

3/31/07 7:01:37 PM

L17	5	I16 and I12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 19:00
L19	216	delay strobe signal\$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:43
L20	1320	delay locked loop circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:44
L21	15	I19 and I20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:44
L22	7	(adjust\$3 or modify\$3 or updat\$3 or chang\$3 or vary\$3 or rearrang\$3) same (duration near1 delay same delayed strobe signal\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:50
L23	2	l21 and l22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:50
L25	37243	714/738 or 714/821 or 714/712 or 714/820 or 714/? or 714/739 or 714/728 or 709/? or 365/201 or 365/? or 375/260 or 375/? or 713/401 or 713/? or 714/700 or 714/707 or 714/731 or 714/744 or 714/775 or 714/798	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/03/31 18:49

3/31/07 7:01:37 PM

L29	4	I21 and I25	US-PGPUB;	ADJ	ON	2007/03/31 19:00
			USPAT;			, .
	•		USOCR;			
ŀ		·	FPRS;	İ		
			EPO; JPO;			
			DERWENT;	İ		
			IBM_TDB			

3/31/07 7:01:37 PM